# Megaprocessor

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Simulator User Guide

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## **1. Introduction**

The simulator for the Megaprocessor is a Windows application It can be downloaded from <u>www.megaprocessor.com</u>. There is also an assembler and some example programs. Program images in Intel Hex format can be loaded and run. The simulation is cycle accurate. Some of the peripherals are emulated including memory, timers and GPIO. (Interrupts and the UART are not currently, May 2016, simulated). Breakpoints and single stepping are possible as well as free running.

TIP:

The "Registers" and "Peripherals" windows are updated as each instruction is executed. This has a significant impact on speed of simulation. This can be reduced if those windows are minimised or closed.

# 2. Instructions

On starting the simulator generates an initial random program and presents a set of windows which will look something like :



To simulate the execution of a particular program use File::Load. This will bring up a File Open dialog to find and select an Intel Hex format file (.hex extension) containing the image you wish to simulate. (This will have been created by the Assembler).

Loading a file will simulate a reset which will set the PC register to zero. The simulation is controlled through the debug menu :



Debug::Run will cause the simulation to execute instructions until either asked to halt, or a breakpoint is executed (see section on Disassembly window), or a memory violation occurs (see section on Registers window).

The simulation can also single step instructions using Debug::Step.

Debug::Reset simulates a reset. The PC is set to its vector base address and the simulated peripherals are also reset.

During simulation a count is kept of the number of times the processor executes an instruction at each address. The set of current counts can be saved to file using Debug::Stats Save. The counts can be cleared to zero using Debug::Stats Reset. This can be useful for performance profiling.

## 3. Windows

#### a. Disassembly

Each time an image is loaded the memory is disassembled. This disassembly can be viewed in a disassembly window.

If the instruction currently pointed to by the PC is in view it will be indicated by a green arrow.

Double clicking on a line will set a breakpoint on it. Double clicking on that line again will clear the breakpoint. Breakpoints are indicated by red circles.

2	Internal	RAM data			
<u>A0</u>	門 Trac	e Log			
AU AO	Acce	ess violation : Wr @	0xE184	0 8404 80	
A0		Disassembly			
AU 10		0000 : 29	XOR	R1, R2	
AU 10	RES	0001 : 23	XOR	R3, R0	
AU		0002 : BE 84 E1	ST.B	0xE184, R2	
AU		<b>&gt;</b> 0005 : 6C	SUB	R0, R3	
AU		🛑 0006 : D6 AE	LD.B	R2, #0xAE	
AU		0008 : 52	ADDQ	R2, #2	
AU		0009 : 90	LD.W	RO, (R2++)	
AU		000A : 49	ADD	R1, R2	
AU		000B : F1	MOVE	SP, RO	
AU		000C : F1	MOVE	SP, RO	
A0		000D : BB E9 EB	ST.W	0xEBE9, R3	
A0		0010 : B3 A6 DB	LD.W	R3, 0xDBA6	
		0013 : 3C	OR	R0, R3	

Right clicking in the disassembly window will bring up a popup dialog:

Goto address	×
Address	
ОК	Cancel

Entering an address (in hexadecimal) will cause the disassembly window to start displaying from that address.

NOTE: The disassembly listing is created when an image is loaded. If you mix code and data you may find that the disassembly is incorrect for the first one or two instructions located immediately after a data section. This is because the disassembler does not know what is what and treats everything as code. (The simulation will execute the correct instructions i.e. what is actually located at the address). This can be avoided by:

- not mixing code and data
- or appending each data section with three NOP opcodes (0xFF).

#### b. Trace Log

Each time an instruction is executed an entry is added to the trace log. These entries give the address and instruction executed as well as the values of the R0, R1, R2, R3, PS and SP registers. If a memory access occured then that is also shown. Entries are also added for a RESET event, and if a memory violation occurred (see section on registers window).

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02	🚆 Trace Lo	9						
02 02 02 02 02 02 02 02 02 02 02 02	Access 2: 1: 0: RESET	violatic 0002 : 1 0001 : 3 0000 : 3	on : Wr 1 BE 84 E1 23 29	₽ 0xE184   ST.B   XOR   XOR	0xE184, R3, R0 R1, R2	R2	R0[CDCD] R1[0000] R2[CDCD] R3[0000] SP[CDCD] P5[C5]    ¥r.CD@E184      R0[CDCD] R1[0000] R2[CDCD] R3[CDCD] SP[CDCD] P5[C5]       R0[CDCD] R1[CDCD] R2[CDCD] R3[CDCD] SP[CDCD] P5[CD]	

## c. External/Internal Ram data

These are windows onto memory.

The Internal RAM window displays the contents of the 256 bytes of memory based at 0xA000 which corresponds to the Megaprocessor RAM built from discrete components.

The External RAM window displays the contents of the 32K bytes of memory based at 0x0000 which corresponds to the RAM built from a RAM chip.

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11	📴 Ext	ern	al RA	M dat	a															I	_ 🗆	×		
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**	01D0	:	7F	70	F0	A7	54	86	32	95	ΑA	5B	68	13	0B	E6	FC	F5						
÷Ŧ	01E0	:	CA	BE	7D	9F	89	88	41	1B	FD	B8	4F	68	F6	72	7B	14						
**	01F0	:	99	CD	D3	0D	FO	44	ЗA	B4	Α6	66	53	33	0B	CB	Α1	10						
÷÷	0200	:	5E	4C	EC	03	4C	73	E6	05	B4	31	0E	AA	AD	CF	D5	BO						1
	0210	:	CA	27	FF	D8	9D	14	4D	F4	79	27	59	42	7C	9C	C1	F8						4
11	0220	:	CD	8C	36	Inte	rnal R	AM da	ata															
<b>1</b>	0230	:	99	上/	: A	000	: 3F	63	81	BC	B9	65	6 A	70	8E	63	50	5D	2D	88	02	21	×	
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Ψ÷.	0270	:	32	34	_] À	030	: CA	0B	A6	EC	45	66	72	35	A5	D8	A8	2E	2F	20	5F	AO		9FD4]
**	0280		88	81	) A	040	: 55	79	33	C6	38	11	EB	5F	6E	BC	59	02	FA	EA	82	82		
ŦŦ	0290	:	0D	92		050	: AH	D7	FF 0.0	82	83	01	A3	9A	80	DF	5E	AB	D6	DU	61	60		0.000.4.1
11	02A0	:	BO	95	ι A λ	070	: BU	52	83	45	68	74	世4 つく	1 1 2	. 9A 64	88	07	이 민준	A4 07	21	<u>Е</u> б 20	EF		9FD4 J
Ξŧ	02B0	:	A5	F6	: A	070	. DA · 15	. 57 93	72	55 174	44	15	20	10	. 04 ೯೧	02	07 95	90 50		84 0C	00 C1	05		GDCD1
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**	02D0	:	84	C6		040	- E8	Å6	FB	81	D3	DC	ÀF	9B	1 H	81	84	F1	40 A9	69	5D	1B		
**	02E0	:	10	50	A	OBO	: 82	16	EF	D4	49	2F	Å1	09	04	2D	52	30	23	58	81	DB		CDCD1
11	02F0	:	31	6C	A	0C0	: BE	F2	B1	8D	1E	B2	12	CC	7F	74	5D	77	14	2E	00	5A		CDCD1
11	0300	:	57	C7	Å	ODO	: 40	26	7B	00	54	62	ΟA	C8	DD	60	84	3B	1F	08	83	9D		CDCD1
**	0310	:	34	4E	j A	0E0	: 1D	DF	C5	C2	2B	7D	D2	24	ΑE	41	DF	32	24	43	F3	ΕA		
11	0320	÷	B8	21	: A	OFO	: 64	8A	48	Α9	26	80	F4	42	C5	A2	C8	4E	44	7C	79	C4		[CDCD]
Ŧ÷	0330		10	D0	1																			[CDCD]
	0340	:	56	6 J																				[CDCD]
22	0360	:	F۵	72	-																			

Double clicking on a byte value will bring up a dialog allowing you to change the value at that location (value in hexadecimal).

Change Memory Value	×
A052 F	
ОК	Cancel

Right clicking will bring up the dialog to enter an address (in hexadecimal) for the window display to start from.

#### d. Peripherals

This window allows the simulation of some of the peripherals. In particular I/O, counter and timer. Interrupts and the UART are not currently (May 2016) simulated.



The timer block simulates the counter and timer. These will update each cycle in the same way as the real hardware does. There is no interaction with these values through the GUI.

The I/O block simulates the modified Venom Arcade Stick attached to the input lines of the Control and I/O frame. (NOTE: on the real hardware there are pullup resistors on all of the input lines. Therefore the default value in real life that will be read is 0xFFFF, and that is simulated here). The

pattern of 5 radio buttons on the left represent the joystick. This is attached to the 4 LS input bits. Selecting one of the outer radio buttons will cause the associated bit to go LOW. Selecting the centre button represents the joystick being centred and all 4 simulated input bits will be HIGH. Bits 4..B represent the 8 buttons (and are labelled the same way). When the checkbox has a cross the bit will read HIGH, when there is no cross the bit will read LOW.



Cycle count is a count of the number of cycles since the last RESET. It does not represent any part of the hardware but is provided for debug. It's a 32 bit counter and so does not wrap as quickly as the simulated counter does.

## e. Registers

This window shows the values of the processor registers and also the memory map.



Double clicking on a register value will bring up a dialog allowing you to change it (new value entered in hexadecimal).

There are some parts of the memory map which in "real life" have no hardware. For debug the simulator can break if they are accessed. In real life the processor will read garbage, and writes will have no effect.

The Megaprocessor can locate its vector table at either 0x0000 or 0xFFF0 and the simulator provides a mechanism to control this. Until I build the ROM frame the only sensible option is 0x0000.

#### f. RAM LEDs

This window shows the contents of the 256 byte RAM built from discrete components as a set of red dots. This is to emulate the appearance of the memory frame. Byte 0 bit 0 is top left (address 0xA000). Top right is byte 3 bit 7.

